

FIG. 1A
PRIOR ART

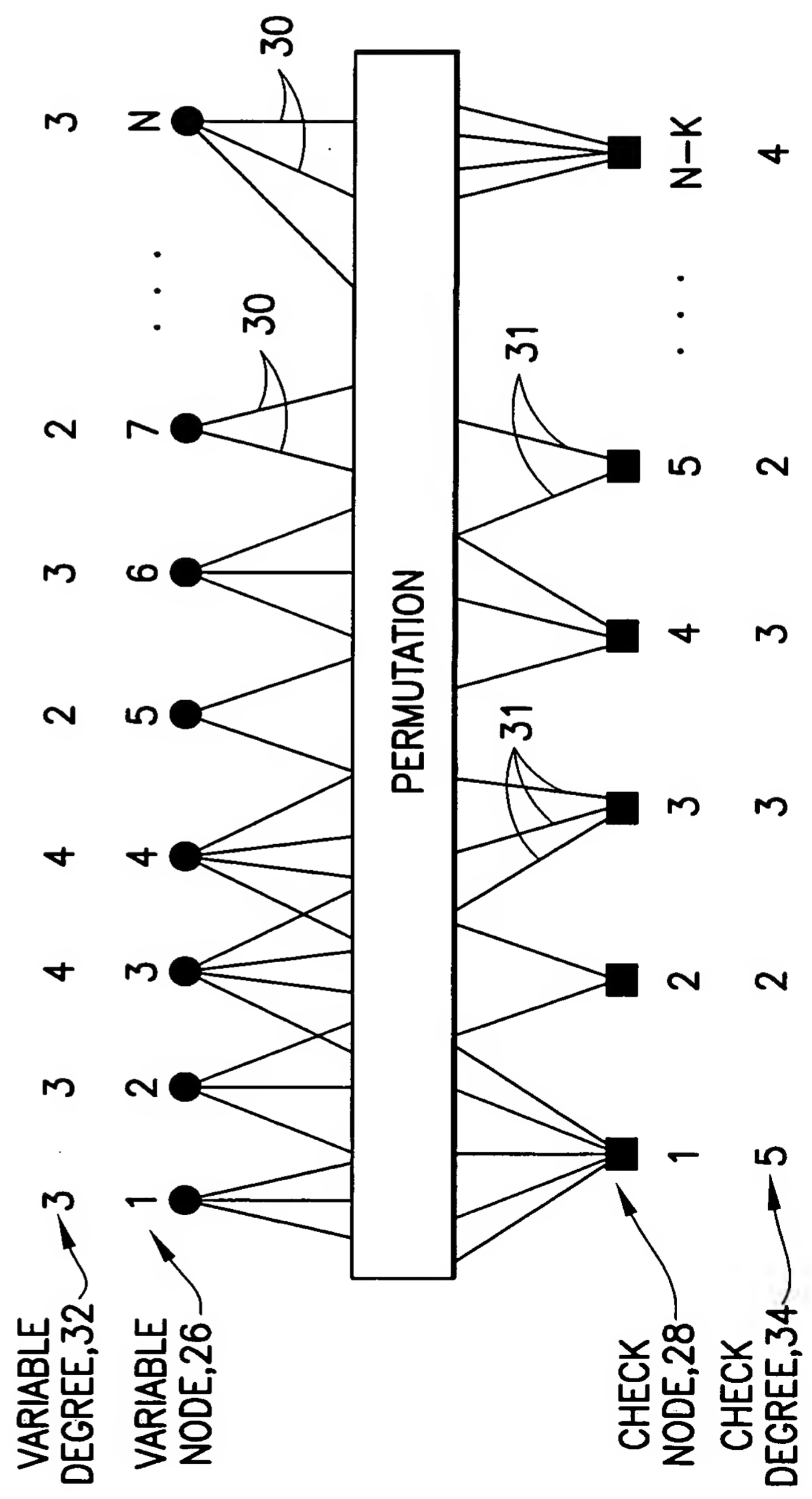


FIG. 1B
PRIOR ART

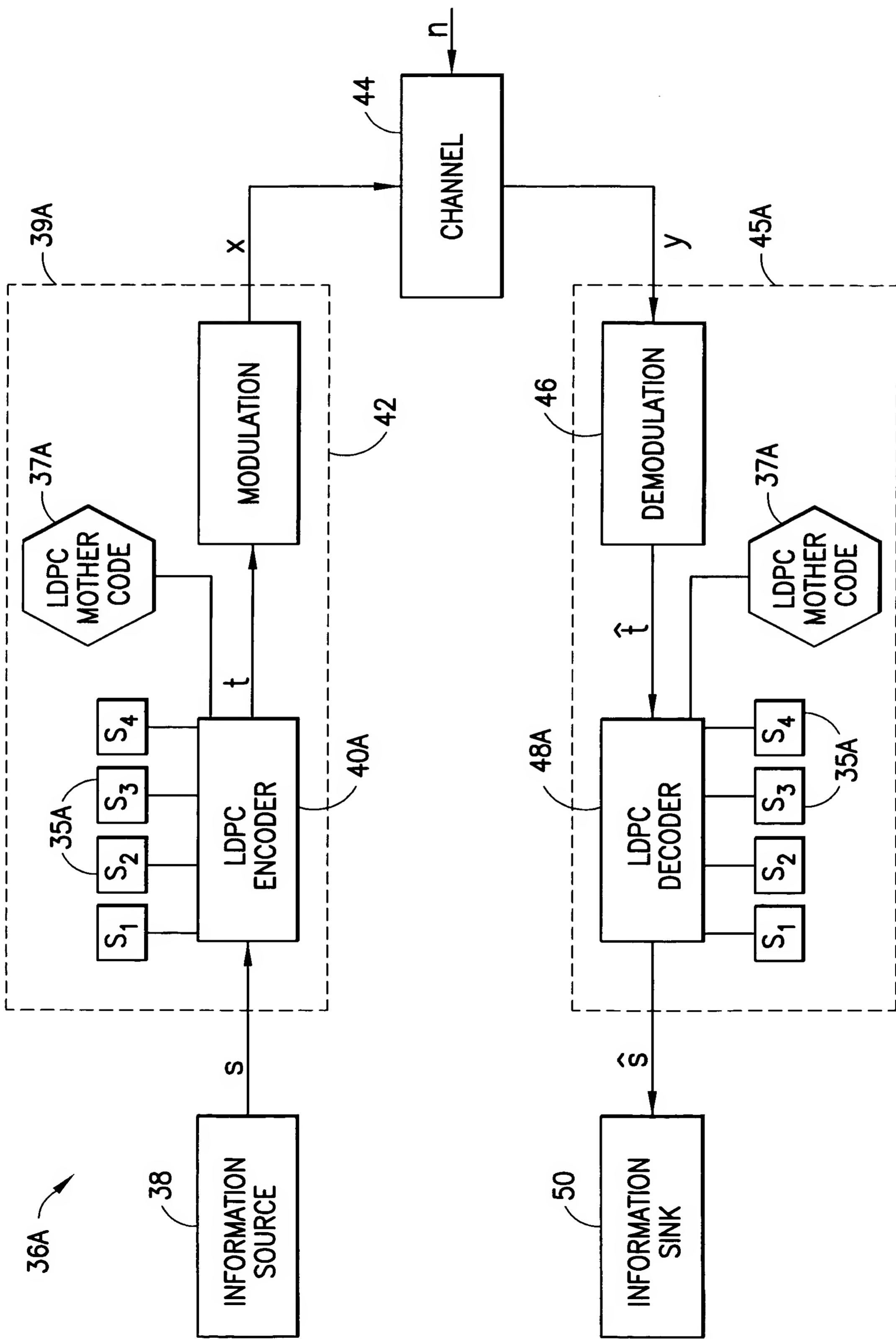


FIG. 2A
PRIOR ART

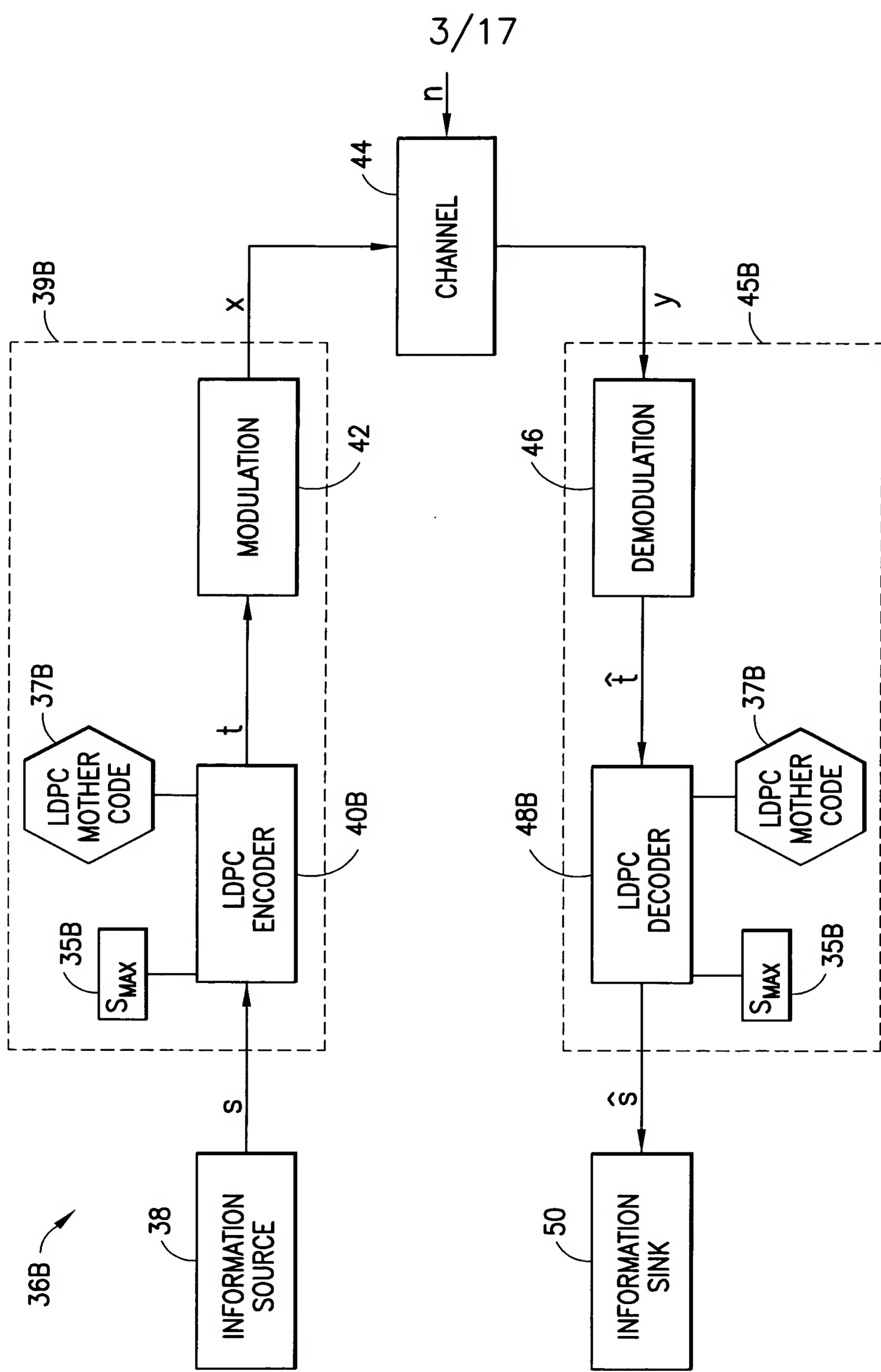


FIG.2B

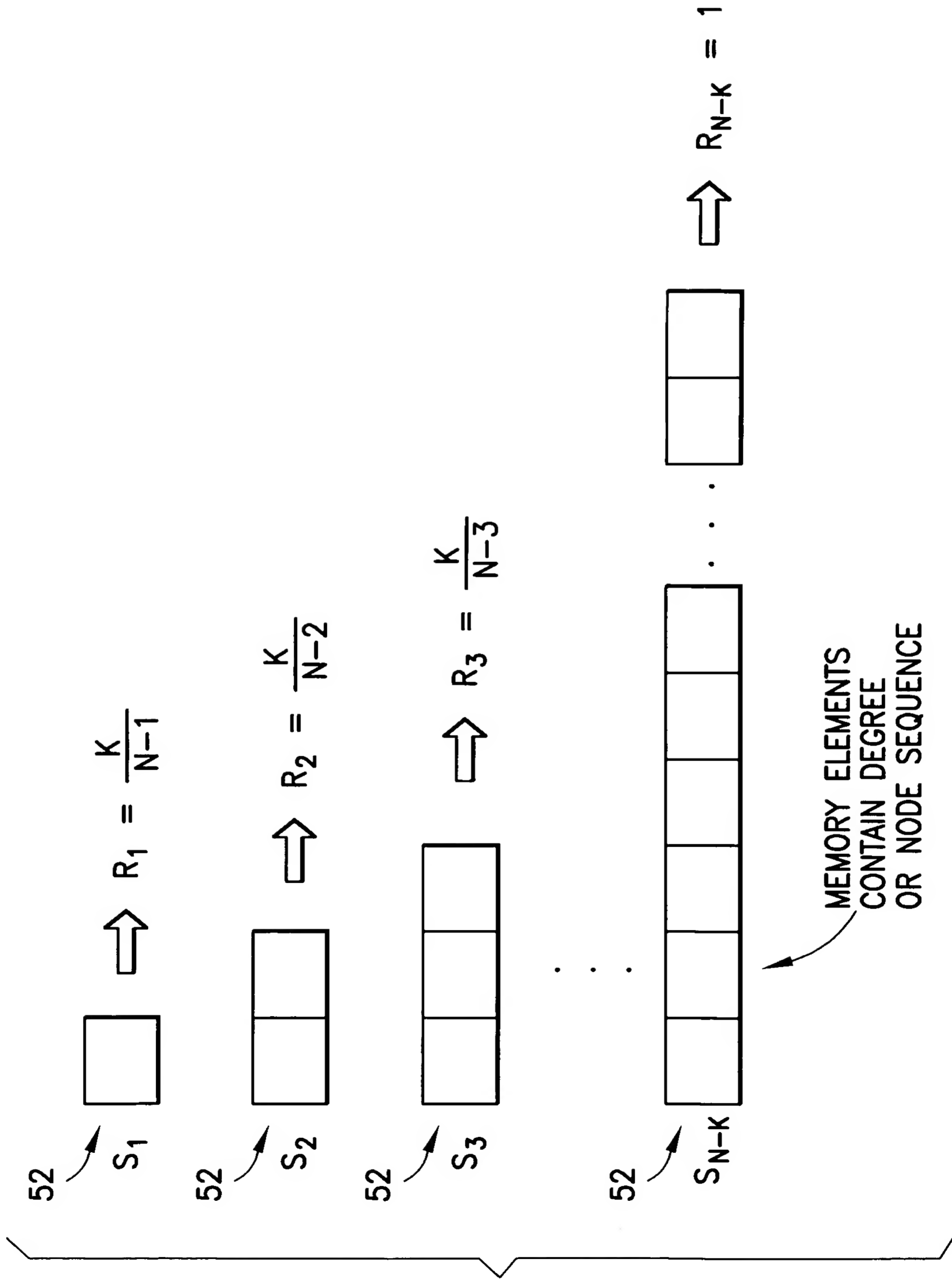


FIG.3
PRIOR ART

$$S_1 \subseteq S_2 \subseteq \dots \subseteq S_{N-K-1} \subseteq S_{N-K}$$

54, MEMORY ELEMENTS
CONTAIN DEGREE
OR NODE SEQUENCE

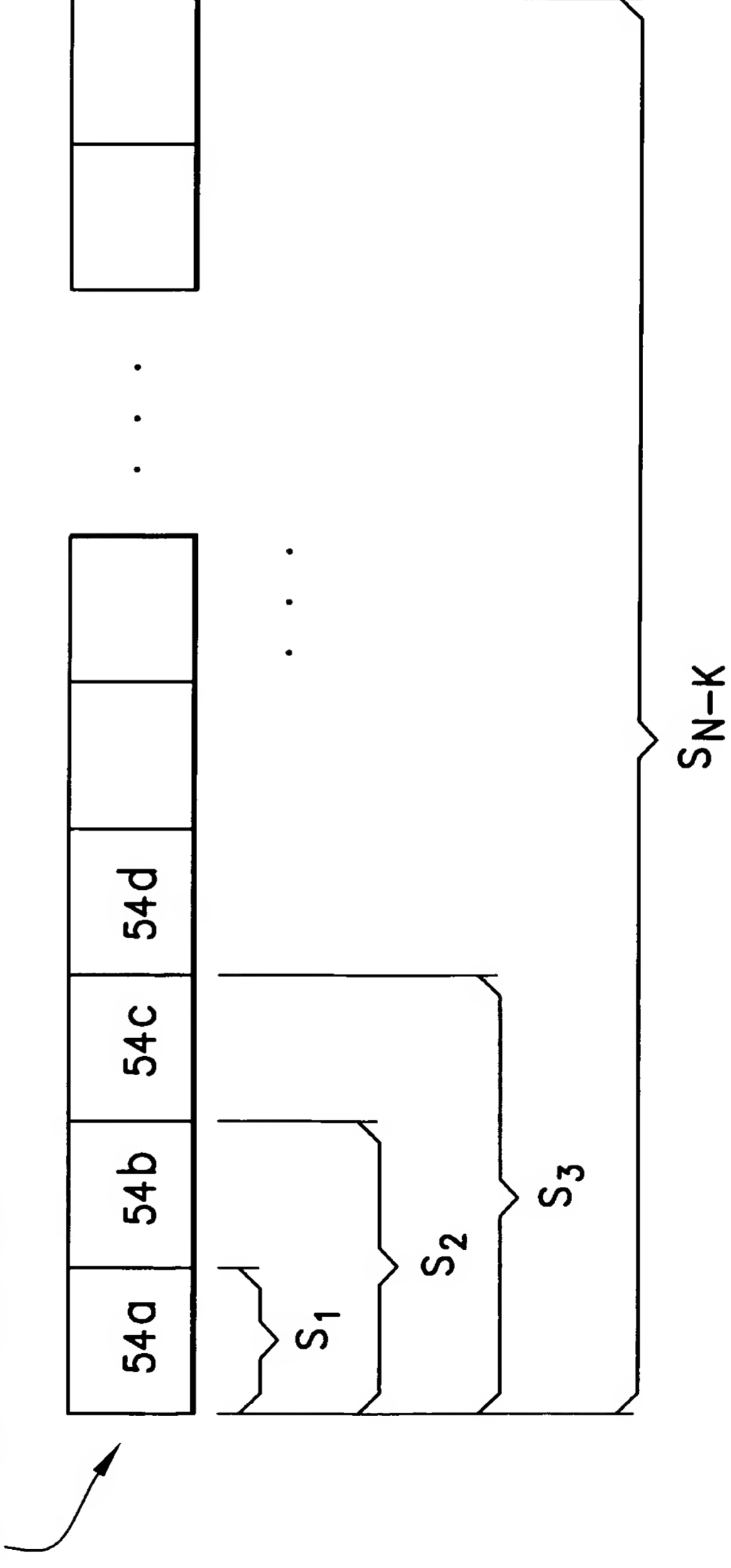


FIG.4

$$\begin{array}{c}
 S_1 \subseteq S_{N-K} \\
 S_2 \subseteq S_{N-K} \\
 \vdots \\
 S_{N-K-1} \subseteq S_{N-K}
 \end{array}$$

54, MEMORY ELEMENTS
CONTAIN DEGREE
OR NODE SEQUENCE

S_3

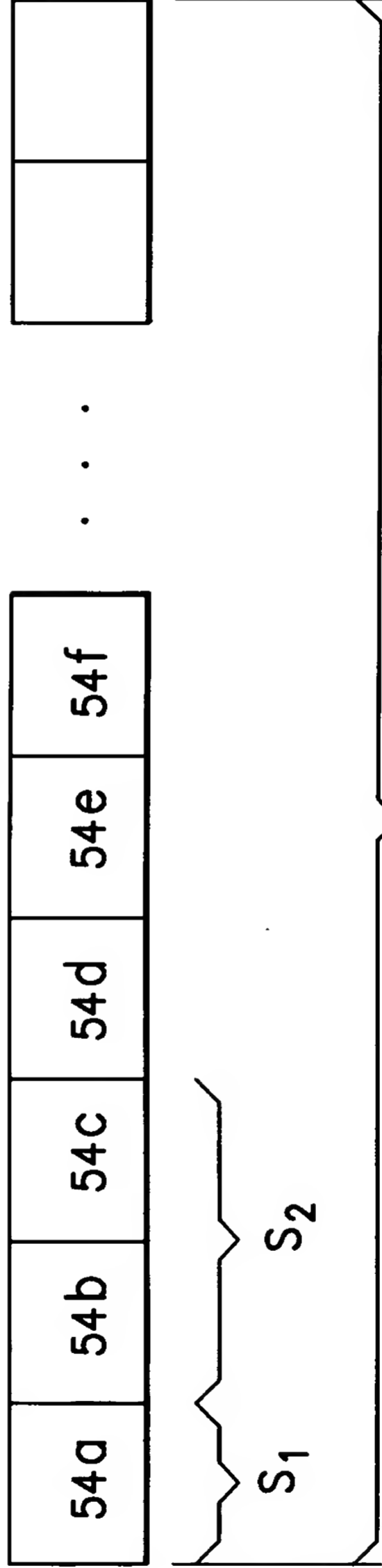


FIG.5

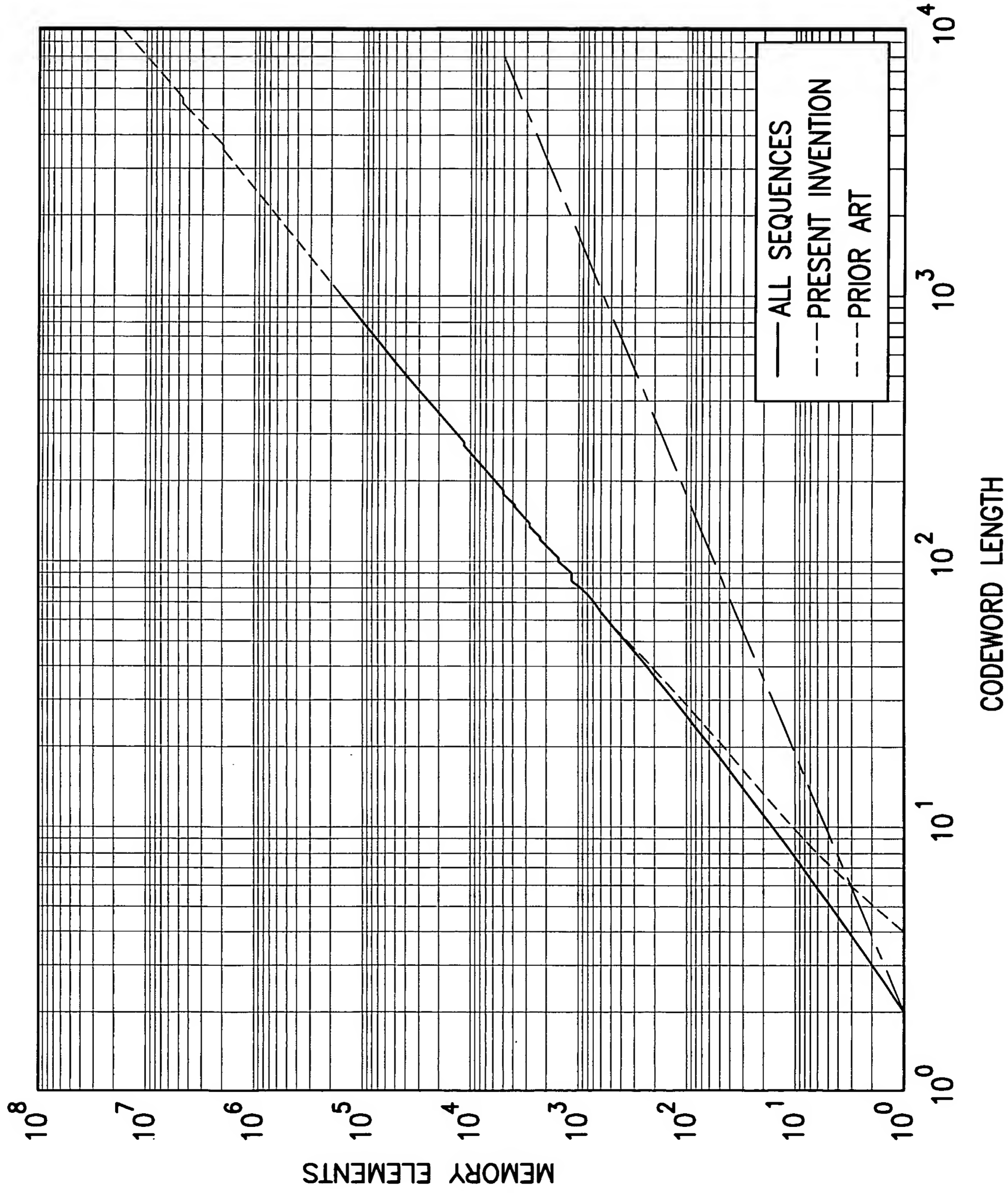


FIG.6

LDPC PUNCTURED N1082 M541CODE12.mat

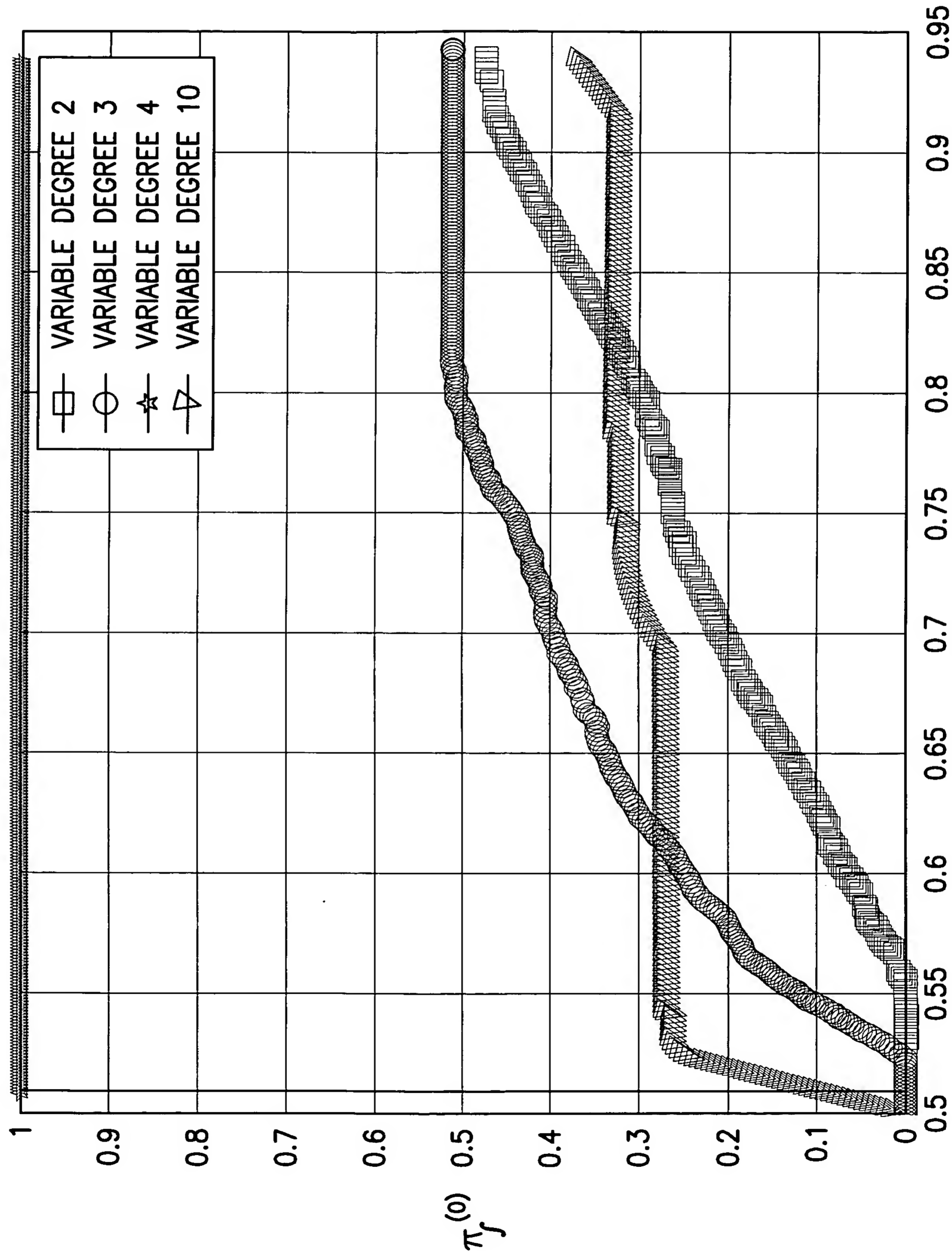
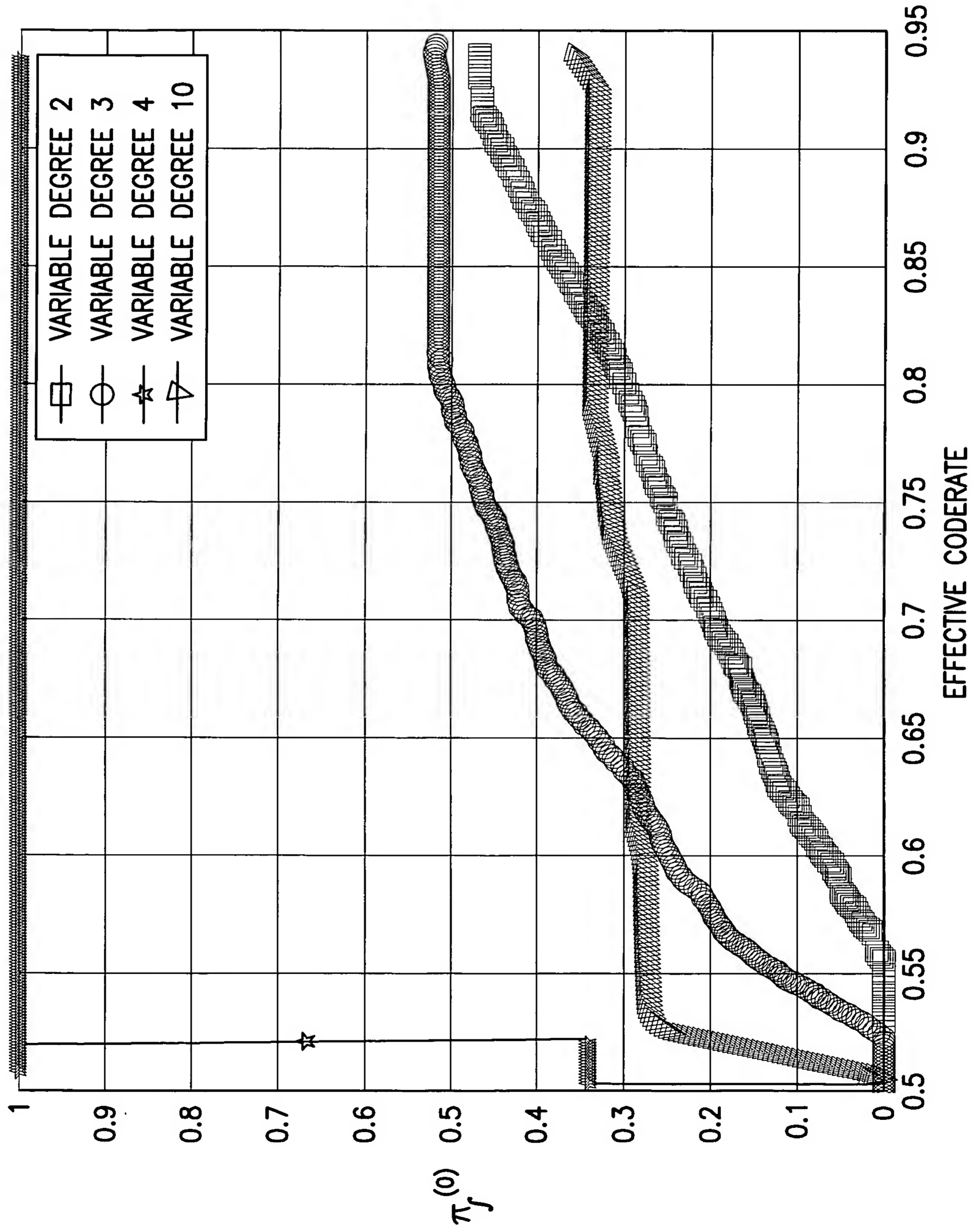


FIG.7

LDPC PUNCTURED N3255 M1627CODE11.mat



SIM OUTPUT N1082 M541CODE12 100iters.mat

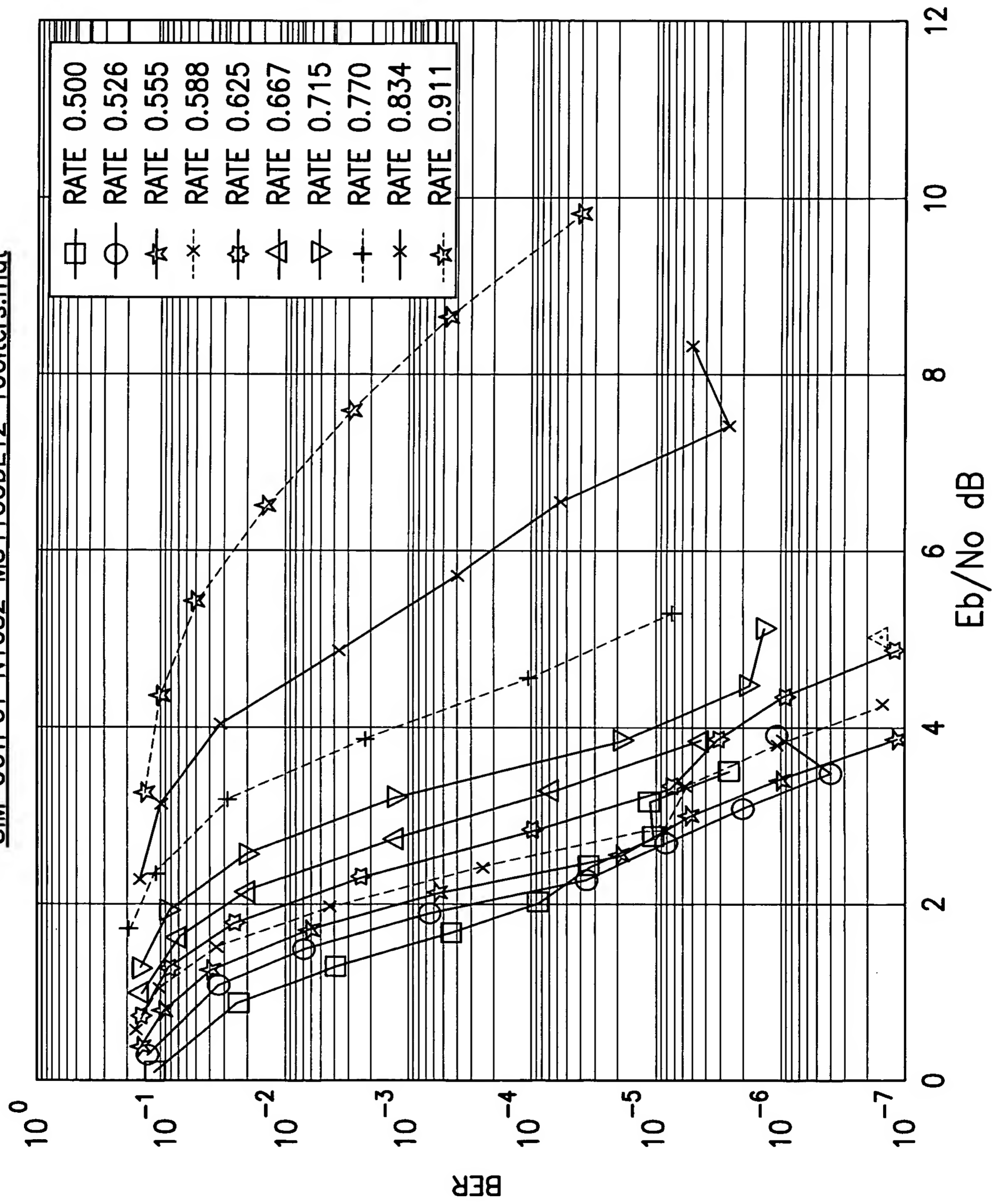


FIG.9

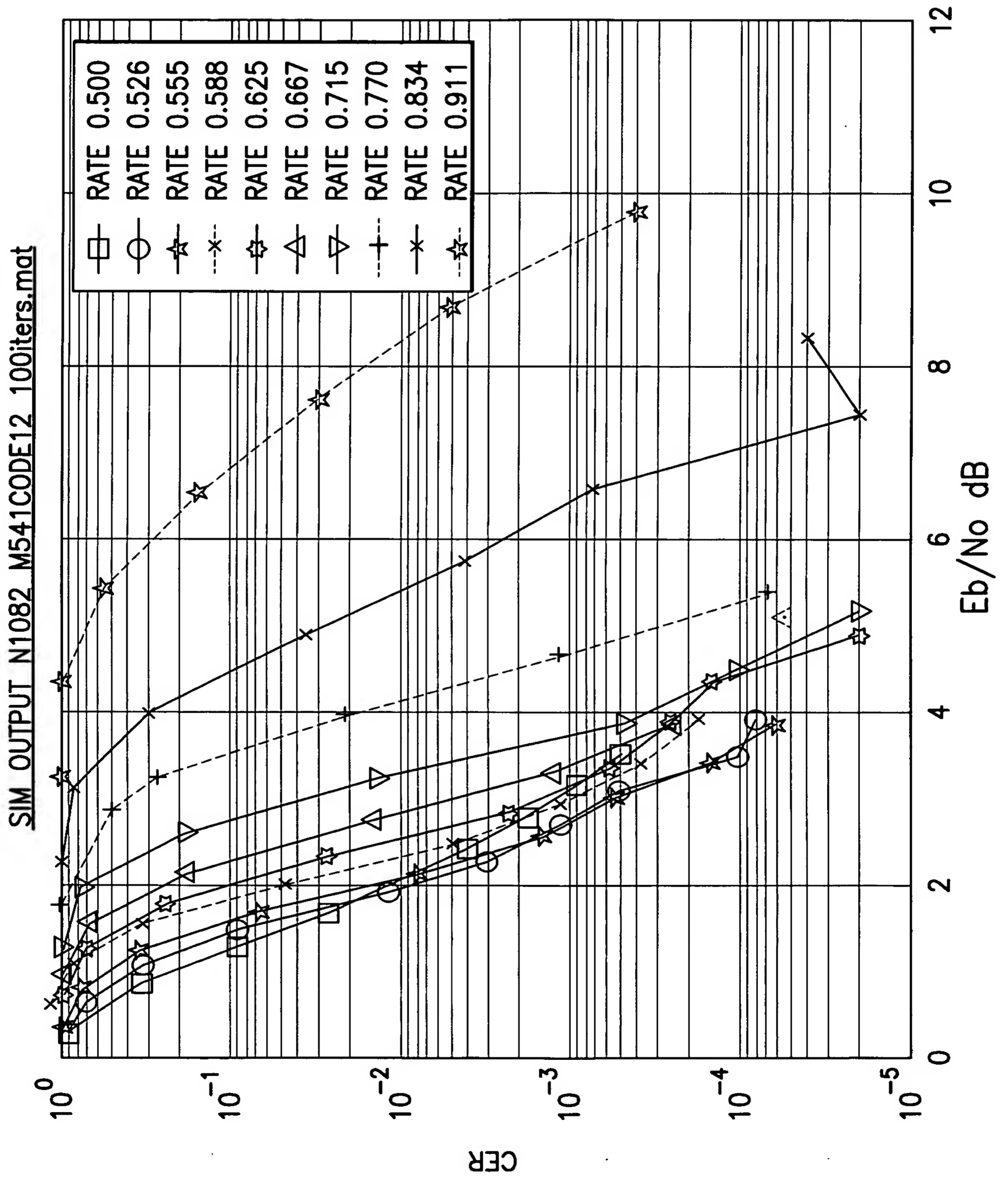


FIG.10

SIM_OUTPUT N1082 M541CODE12 100iters.mat

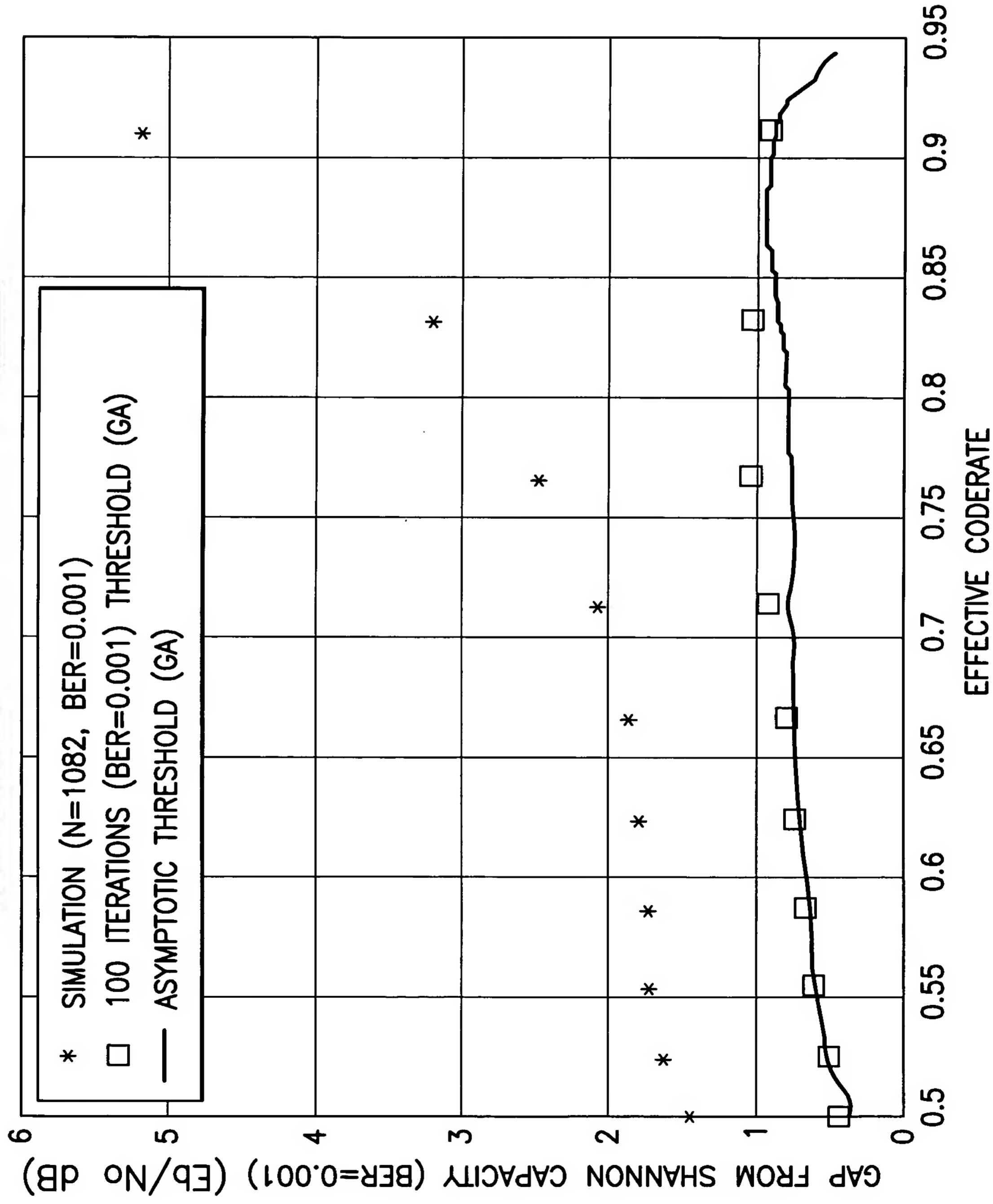


FIG.11

SIM OUTPUT N1082 M541CODE12 100iters.mat

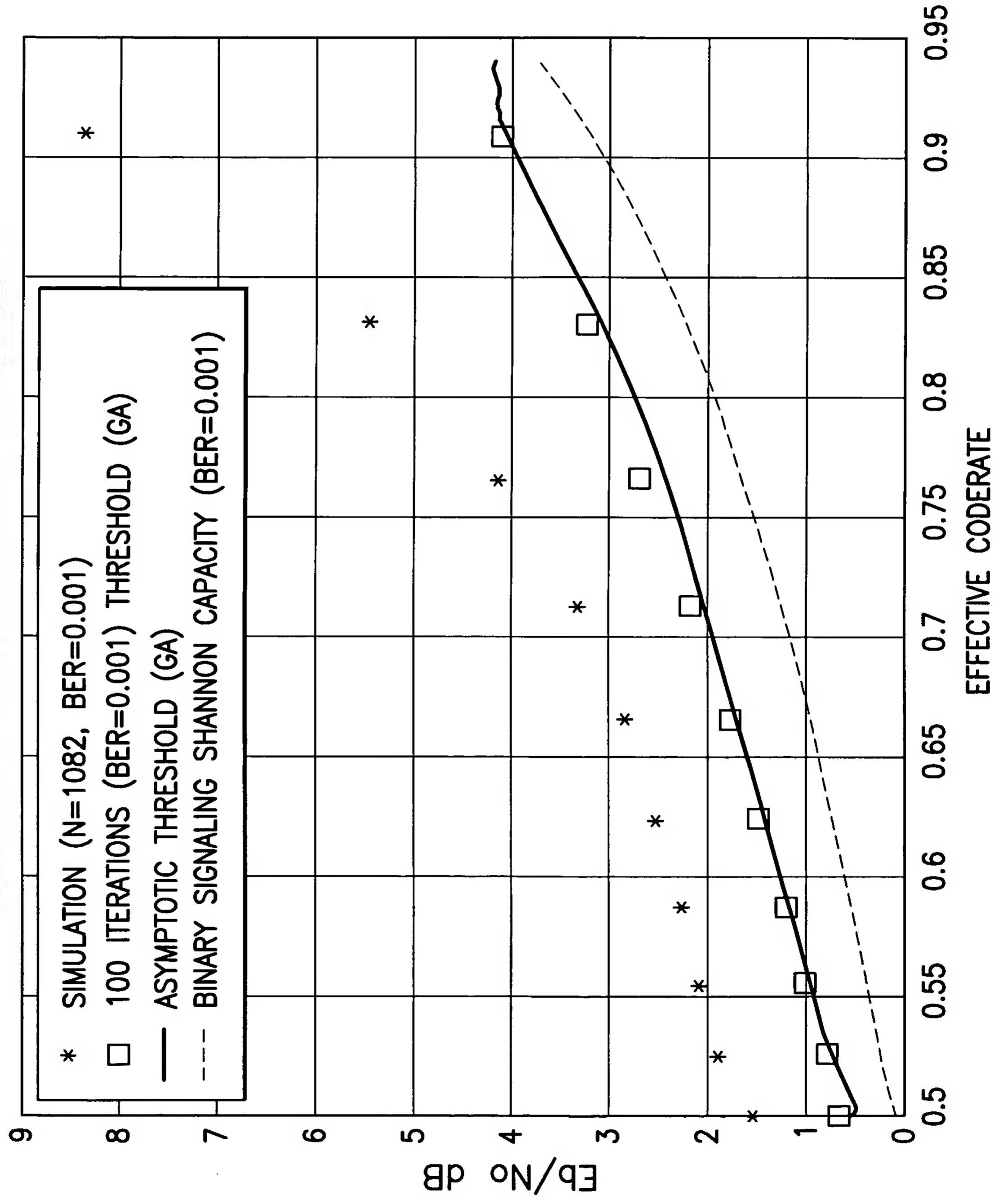


FIG.12

SIM OUTPUT N3255 M1627CODE11 100iters.mat

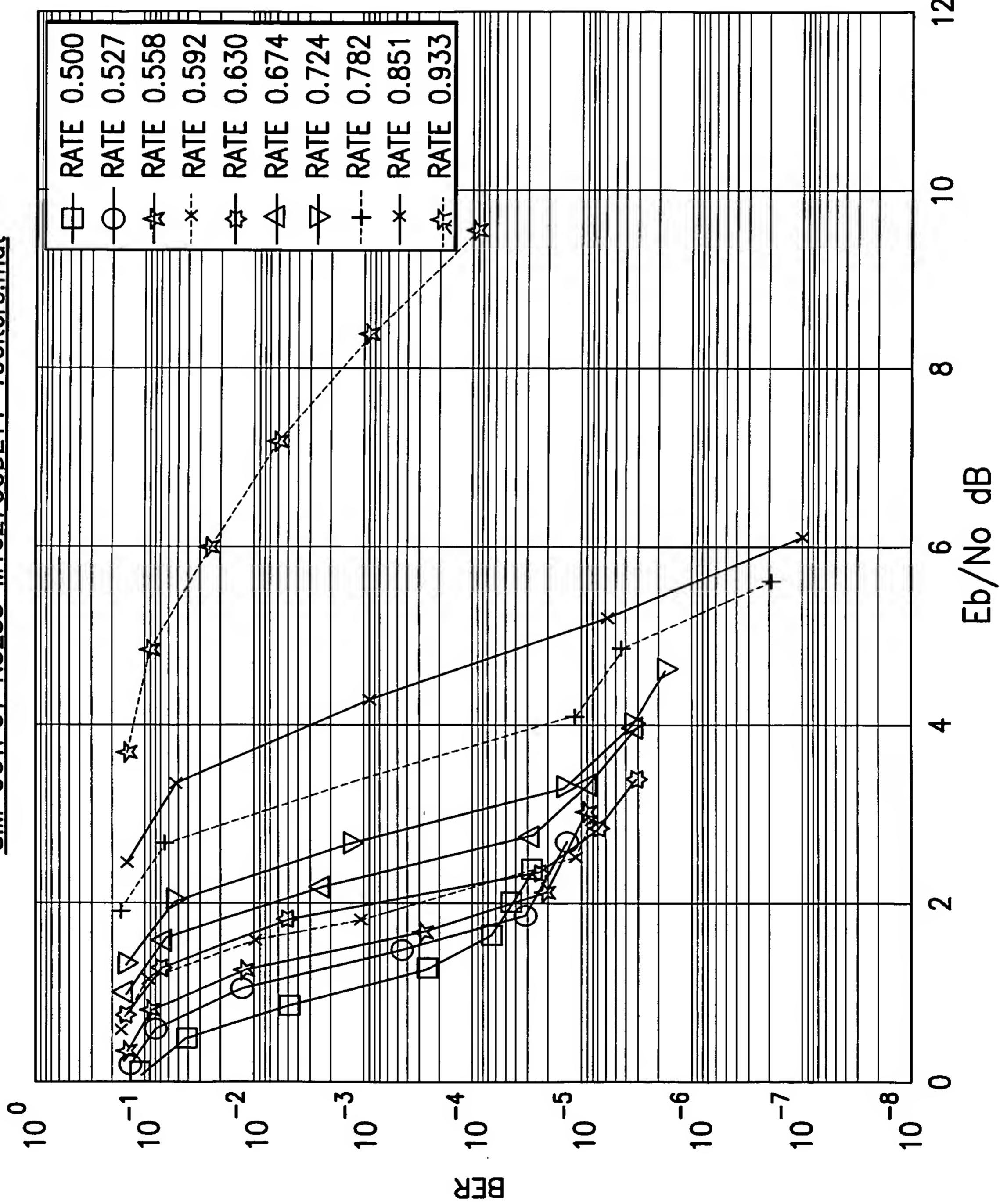


FIG.13

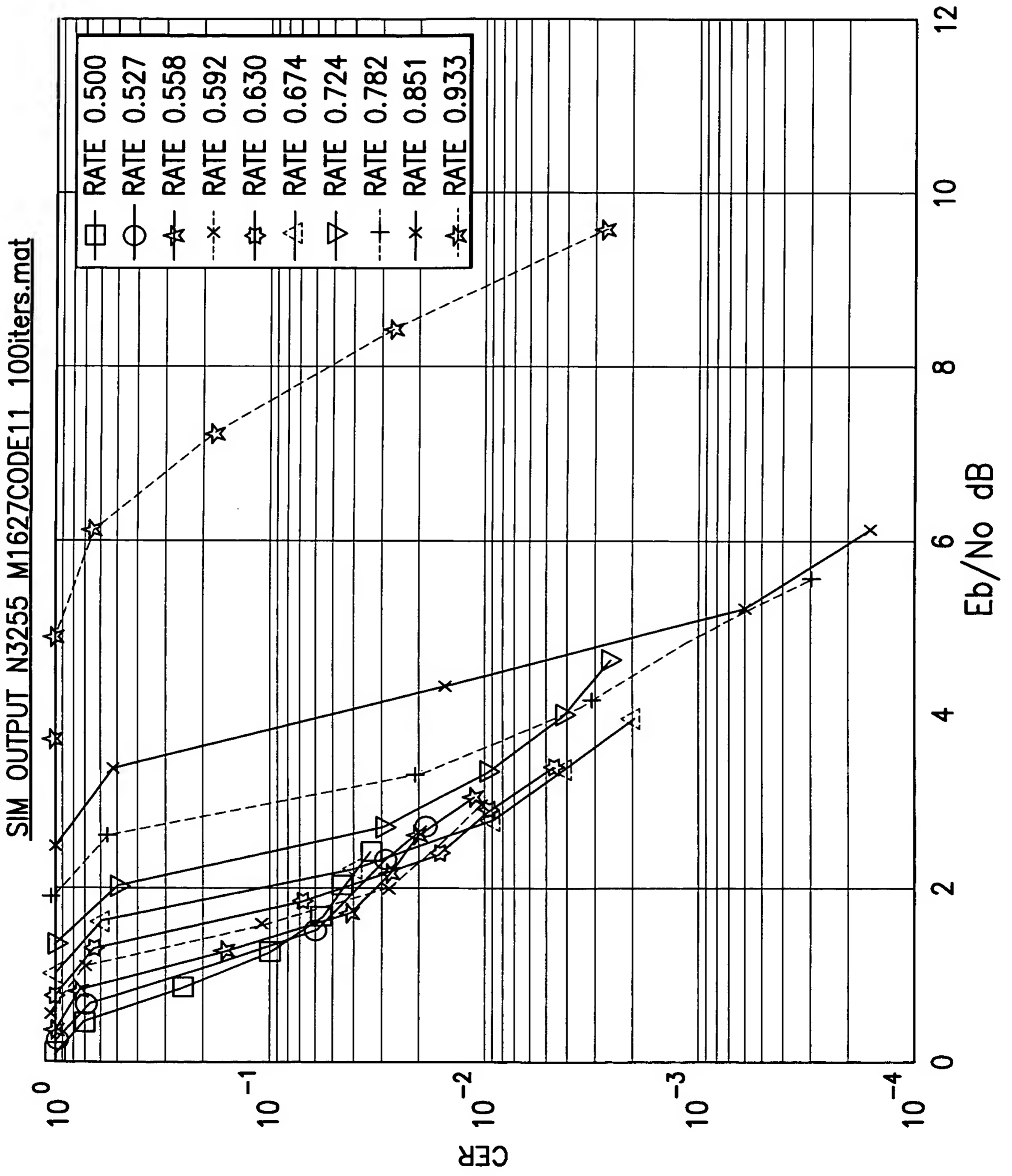


FIG.14

SIM OUTPUT N3255 M1627CODE11 100iters.mat

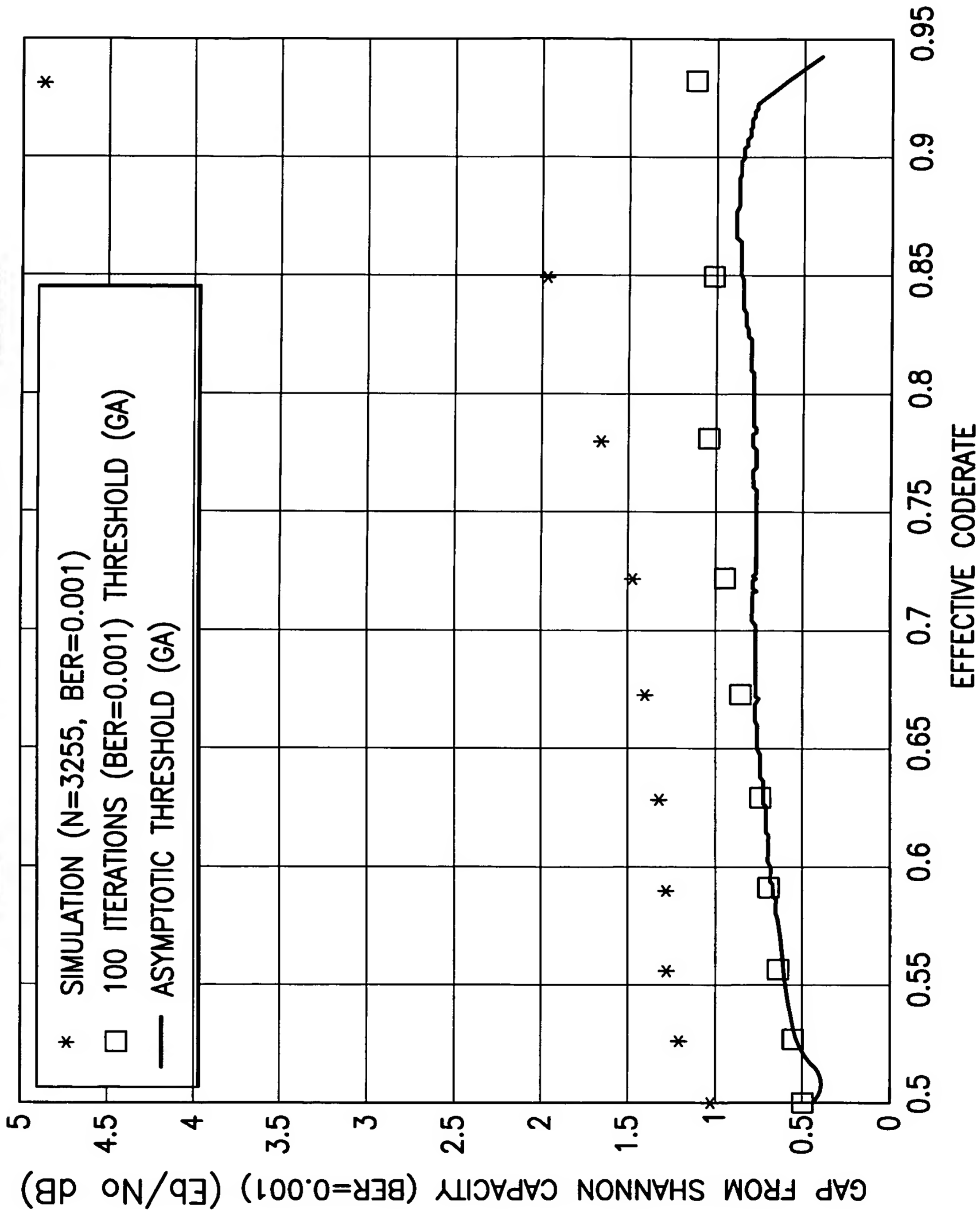


FIG.15

SIM OUTPUT N3255 M1627CODE11 100iters.mat

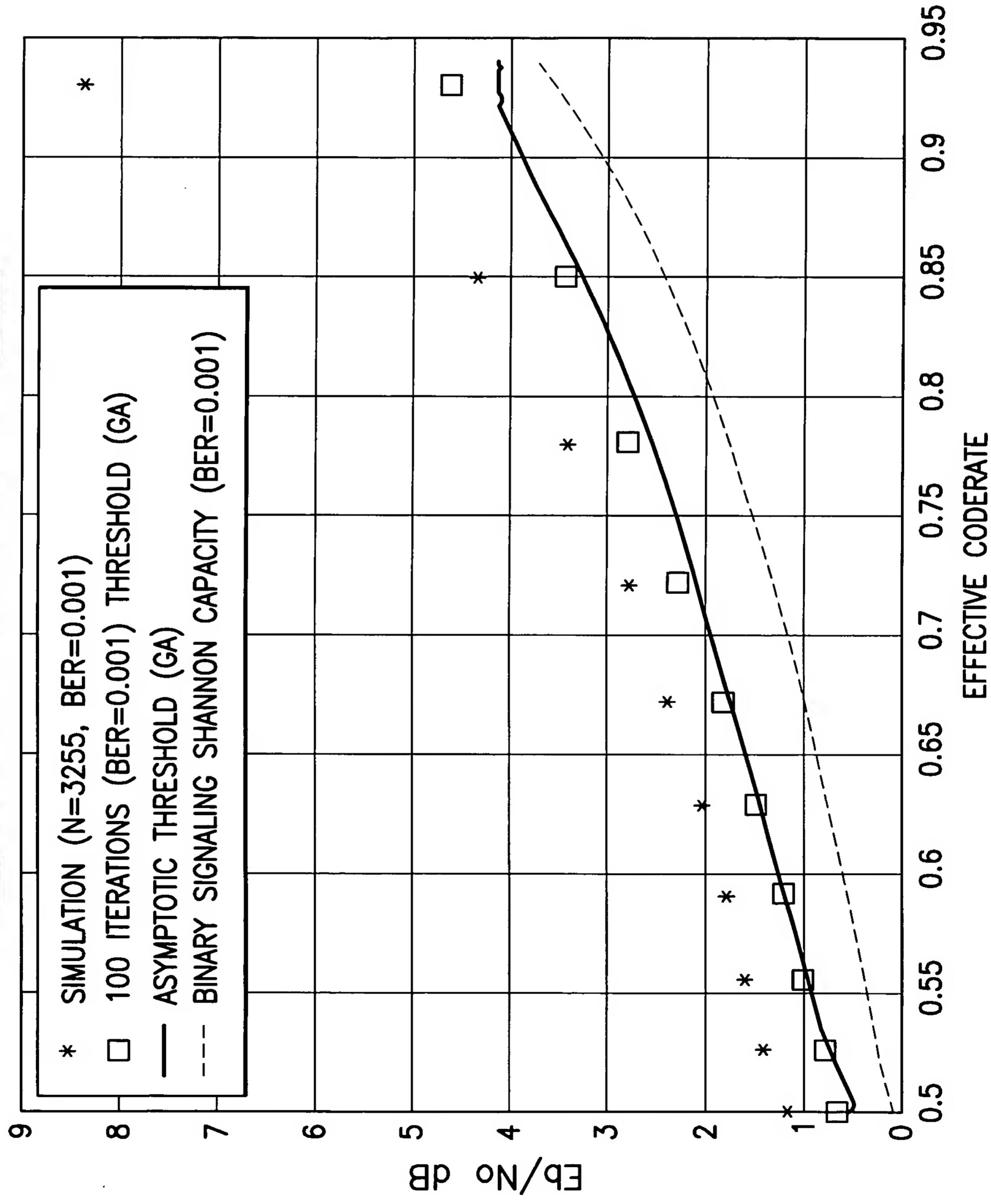


FIG.16